STC5230
Synchronous Clock for SETS
Data Sheet

Description

The STC5230 is a single chip solution of timing source in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813, and Telcordia GR1244, and GR253.

The STC5230 accepts 12 reference inputs and generates 9 independent synchronized output clocks. Reference input frequencies are automatically detected, and inputs are individually monitored for quality. Active reference selection may be manual or automatic. All reference switches are hitless. Synchronized outputs may be programmed for a wide variety of SONET and SDH as well as Synchronous Ethernet frequencies.

Two independent timing generators, T0 and T4, provide the essential functions for Synchronous Equipment Timing Source (SETS). Each timing generator includes a DPLL (Digital Phase-Locked Loop), which may operate in the Freerun, Synchronized, and Holdover modes. Both timing generators support master/slave operation for redundant applications. The proprietary **SyncLink™** cross-couple data link provides master/slave phase information and state data to ensure seamless side switches.

A standard SPI serial bus interface provide access to the STC5230's comprehensive, yet simple to use internal control and status registers. The device operates with an external OCXO or TCXO as its MCLK at 20 MHz.

The STC5230 is capable of field upgrade with optional external EEPROM or via the bus interface.

Features

- For SDH SETS, SONET Stratum 3, 4E, 4 and SMC, and Synchronous Ethernet
- Two timing generators, T0 and T4, for SETS
- Complies with ITU-T G.813, Telcordia GR1244 and GR253
- Supports Master/Slave redundant application with the **SyncLink™** cross-couple data links
- Accepts 12 individual clock reference inputs
- Reference clock inputs are automatically frequency detected; each is monitored for quality
- Support manual and automatic reference selection
- T0 and T4 have independent reference lists and priority tables for automatic reference selection
- Output 9 synchronized clocks
- Could compensate the phase delay of the cross-couple links, in 0.1ns steps up to 409.5ns
- Capable to trace the round-trip phase delay of the master/slave cross-couple links.
- Hit-less reference and master/slave switching
- Phase rebuild on re-lock and reference switches
- Programmable loop bandwidth of each DPLL of the T0 and T4 timing generator, from 90mHz to 107Hz
- Supports SPI bus interface
- Field upgrade capability
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package

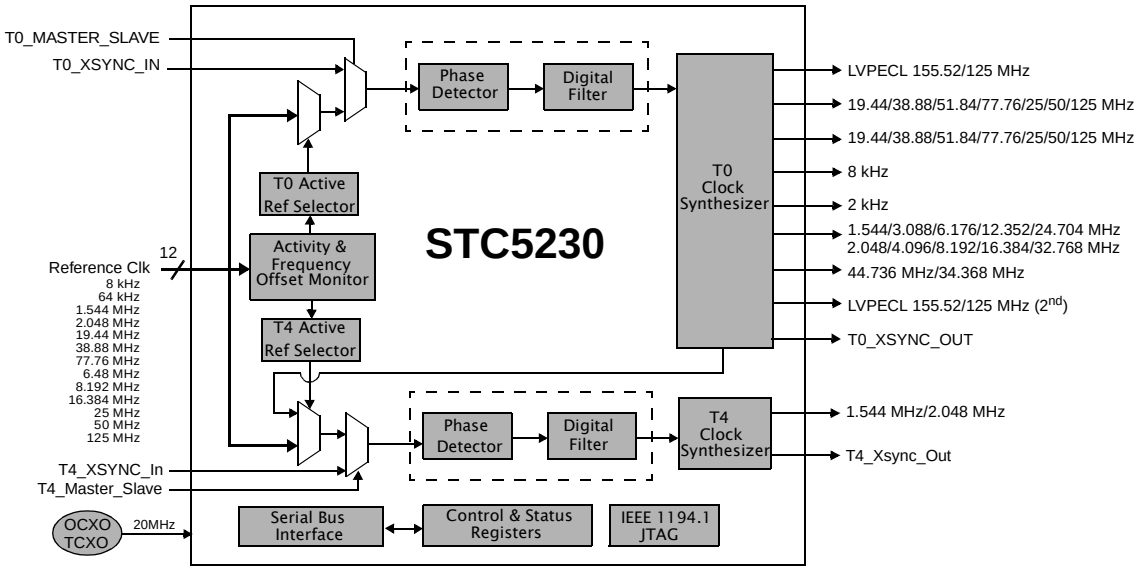
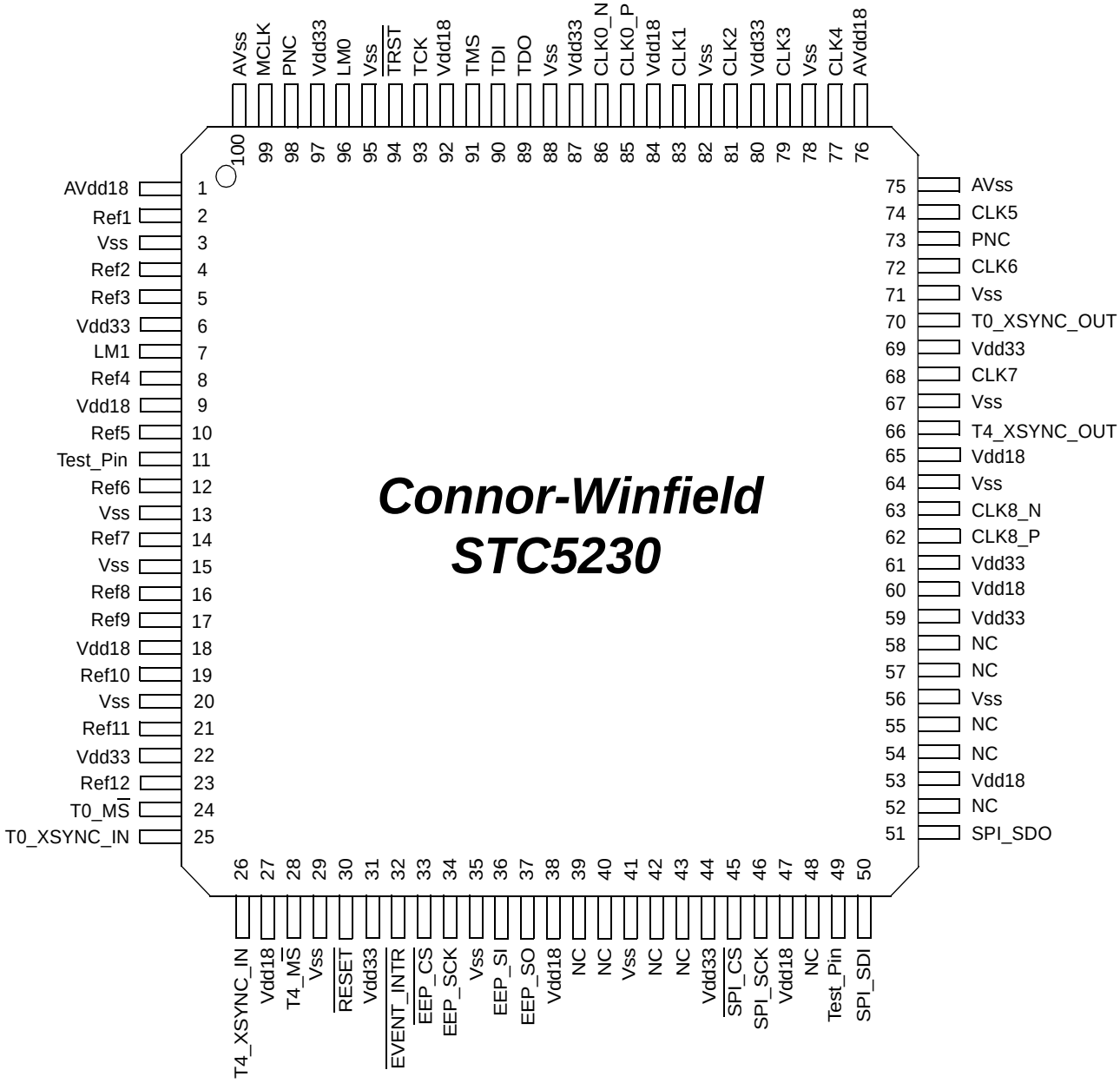


Figure 1: Functional Block Diagram

Table of Contents

Table of Figures

STC5230 Pin Diagram (Top View)



Note: Pins labeled “Test Pin” must be grounded.

STC5230 Pin Description

All I/O is LVCMOS, except for CLK0 and CLK8, which are LVPECL.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
Vdd33	6,22,31, 44,59,61, 69,80, 87,97		3.3V power input
Vdd18	9,18,27, 38,47,53, 60,65,84, 92		1.8V power input
Vss	3,13,15, 20,29,35, 41,56,64, 67,71,78, 82,88,95		Digital ground
AVdd18	1, 76		1.8V analog power input
AVss	75, 100		Analog ground
$\overline{\text{TRST}}$	94	I	JTAG boundary scan reset, active low
TCK	93	I	JTAG boundary scan clock
TMS	91	I	JTAG boundary scan mode selection
TDI	90	I	JTAG boundary scan data input
TDO	89	O	JTAG boundary scan data output
$\overline{\text{RESET}}$	30	I	Active low to reset the chip
MCLK	99	I	Master clock input, 20 MHz
$\overline{\text{SPI\_CS}}$	45	I	SPI bus chip select ($\overline{\text{CS}}$)
SPI_SCK	46	I	SPI bus clock input (SCLK)
SPI_SDI	50	I	SPI bus data input (SDI)
SPI_SDO	51	O	SPI bus data output (SDO)
EEP_SO	37	I/O	Optional external EEPROM SO
EEP_SI	36	I/O	Optional external EEPROM SI
EEP_SCK	34	I/O	Optional external EEPROM SCK
$\overline{\text{EEP\_CS}}$	33	I/O	Optional external EEPROM $\overline{\text{CS}}$
$\overline{\text{EVENT\_INTR}}$	32	O	event interrupt
REF1	2	I	Reference input 1
REF2	4	I	Reference input 2
REF3	5	I	Reference input 3
REF4	8	I	Reference input 4
REF5	10	I	Reference input 5
REF6	12	I	Reference input 6

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
REF7	14	I	Reference input 7
REF8	16	I	Reference input 8
REF9	17	I	Reference input 9
REF10	19	I	Reference input 10
REF11	21	I	Reference input 11
REF12	23	I	Reference input 12
T0_M/$\overline{S}$	24	I	Select master or slave mode for T0, 1: Master, 0: Slave
T4_M/$\overline{S}$	28	I	Select master or slave mode for T4, 1: Master, 0: Slave
T0_XSYNC_IN	25	I	Cross-couple **SyncLink™** data link input for T0 for master/slave redundant applications
T0_XSYNC_OUT	70	O	Cross-couple **SyncLink™** data link output for T0 for master/slave redundant applications
T4_XSYNC_IN	26	I	8kHz cross-couple link input for T4 for master/slave redundant applications
T4_XSYNC_OUT	66	O	8kHz cross-couple link output for T4 for master/slave redundant applications
CLK0_P	85	O[1]	155.52/125 MHz LVPECL output (T0)
CLK0_N	86	O[1]	155.52/125 MHz LVPECL output (T0)
CLK1	83	O	19.44/38.88/51.84/77.76/25/50/125 MHz (T0)
CLK2	81	O	19.44/38.88/51.84/77.76/25/50/125 MHz (T0)
CLK3	79	O	8 kHz frame pulse or 50% duty cycle clock (T0)
CLK4	77	O	2 kHz frame pulse or 50% duty cycle clock (T0)
CLK5	74	O	44.736/34.368 MHz (T0)
CLK6	72	O	1.544/3.088/6.176/12.352/24.704/2.048/4.098/8.192/16.384/32.768 MHz (T0)
CLK7	68	O	1.544/2.048 MHz (T4)
CLK8_P	62	O[1]	155.52/125 MHz LVPECL output (T0)
CLK8_N	63	O[1]	155.52/125 MHz LVPECL output (T0)
LM0	96	I	Hardware and firmware configuration data load mode pin 0
LM1	7	I	Hardware and firmware configuration data load mode pin 1
NC	39,40,42, 43,48,52, 54,55,57, 58		No connection. Pins are recommented to be tied to ground
PNC	73,98		No connection. Pins can be left open, floating, tied up, or grounded
Test_Pin	11,49	I	Test pins, must be grounded for normal operation

Note 1: CLK0 and CLK8, which are LVPECL

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max	Units	Notes
Vdd33	Logic power supply voltage, 3.3V	-0.5	4.5	volts	2
Vdd18	Logic power supply voltage, 1.8V	-0.5	2.5	volts	2
AVdd18	Analog power supply voltage, 1.8V	-0.5	2.5	volts	2
VIN	Logic input voltage	-0.5	5.5	volts	2
TSTG	Storage Temperature	-65	150	°C	2

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Operating Conditions and Electrical Characteristics

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol	Parameter		Min.	Nominal	Max.	Units	Notes
Vdd33	3.3V digital power supply voltage		3.0	3.3	3.6	Volts	
Vdd18	1.8V digital power supply voltage		1.65	1.8	1.95	Volts	
AVdd18	1.8V analog power supply voltage		1.65	1.8	1.95	Volts	
CIN	Input capacitance			8		pF	
TRIP	Input reference signal positive pulse width		10			ns	
TRIN	Input reference signal negative pulse width		10			ns	
TA	Operating Ambient Temperature Range (Commercial)		0		70	°C	
TA	Operating Ambient Temperature Range (Industrial)		-40		85	°C	
Icc (Vcc)	3.3V digital supply current			TBD		mA	
Icc (AVcc)	3.3V analog supply current			TBD		mA	
Pd	Device power dissipation			TBD		W	
VIH (3.3V)	LVCMOS	High level input voltage	2.0		5.5	Volts	3
VIL (3.3V)		Low level input voltage	-0.3		0.8	Volts	3
VOH (3.3V)		High level output voltage (IOH = -12mA)	2.4			Volts	3
VOL (3.3V)		Low level output voltage (IOL =12mA)			0.4	Volts	3
V_T		Threshold point	1.45	1.58	1.74	Volts	3
I_L		Input Leakage Current	-10		10	uA	3

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol	Parameter		Min.	Nominal	Max.	Units	Notes
Voh	LVPECL	Output voltage high	Vdd33 - 1.11		Vdd33 - 0.67	Volts	
Vol		Output voltage low	Vdd33 - 2.0		Vdd33 - 1.4	Volts	
Vod		Output differential voltage	0.8		2.66	Volts	4

Note 3: LVCMOS 3.3 compatible
Note 4: 50 ohms termination to 1.3 (= Vdd33 - 2.0) volts

Register Map

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID, 0x5230
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision
0x04	T0_T4_MS_Sts	1-0	R	Indicates master/slave state
0x05	T0_Slave_Phase_Adj	11-0	R/W	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps
0x07	T4_Slave_Phase_Adj	11-0	R/W	Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps
0x09	Fill_Obs_Window	3-0	R/W	Leaky bucket fill observation window, 1 ~ 16 ms
0x0a	Leak_Obs_Window	3-0	R/W	Leaky bucket leak observation window, 1 ~ 16 times the Fill_Obs_Window
0x0b	Bucket_Size	5-0	R/W	Leaky bucket size, 0 ~ 63
0x0c	Assert_Threshold	5-0	R/W	Leaky bucket alarm assert threshold, 1 ~ 63
0x0d	De_Assert_Threshold	5-0	R/W	Leaky bucket alarm de-assert threshold, 0 ~ 62
0x0e	Freerun_Cal	10-0	R/W	Freerun calibration, - 102.4 ~ + 102.3 ppm
0x10	Disqualification_Range	9-0	R/W	Reference disqualification range (pull-in range), 0 ~ 102.3 ppm
0x12	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~ 102.3 ppm
0x14	Qualification_Timer	5-0	R/W	Reference qualification timer, 0 ~ 63 s
0x15	Ref_Selector	3-0	R/W	Determines which reference data is shown in register 0x16
0x16	Ref_Frq_Offset	15-0	R	Reference frequency and frequency offset of the reference selected by register 0x15
0x18	Refs_Activity	13-0	R	Reference and cross reference activity
0x1a	Refs_Qual	11-0	R	Reference 1 ~ 12 qualification
0x1c	T0_Control_Mode	5-0	R/W	OOP -Follow/Don't Follow, Manual/Auto, Revertive, HO_Usage, PhaseAlignMode
0x1d	T0_Bandwidth	4-0	R/W	Loop bandwidth selection
0x1e	T0_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x1f	T0_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x20	T0_Device_Holdover_History	31-0	R	Device Holdover History for T0 relative to MCLK
0x24	T0_Long_Term_Accu_History	31-0	R	Long term Accumulated History for T0 relative to MCLK
0x28	T0_Short_Term_Accu_History	31-0	R	Short term Accumulated History for T0 relative to MCLK
0x2c	T0_User_Accu_History	31-0	R/W	User Holdover data for T0 relative to MCLK
0x30	T0_History_Ramp	6-0	R/W	Bits 6-4, Long term history accumulation bandwidth: 9.7, 4.9, 2.4, 1.2, 0.61, 0.03 mHz Bits3-2, Short term history accumulation bandwidth: 2.5, 1.24, 0.62, 0.31 Hz Bits 1-0, Ramp control: none, 1, 1.5, 2 ppm/s
0x31	T0_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode, 4 bits/reference
0x37	T0_PLL_Status	7-0	R	OOP, LOL, LOS, Sync, HHA, AHR, SAP
0x38	T0_Accu_Flush	0-0	W	0: Flush/reset the long-term history, 1: Flush/reset both the long-term and the device holdover history
0x39	T4_Control_Mode	5-0	R/W	OOP -Follow/Don't Follow, Manual/Auto, Revertive, HO_Usage, PhaseAlignMode
0x3a	T4_Bandwidth	4-0	R/W	Loop bandwidth selection
0x3b	T4_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x3c	T4_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x3d	T4_Device_Holdover_History	31-0	R	Device Holdover History for T4 relative to MCLK

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x41	T4_Long_Term_Accu_History	31-0	R	Long term Accumulated History for T4 relative to MCLK
0x45	T4_Short_Term_Accu_History	31-0	R	Short term Accumulated History for T4 relative to MCLK
0x49	T4_User_Accu_History	31-0	R/W	User Holdover data for T4 relative to MCLK
0x4d	T4_History_Ramp	6-0	R/W	Bits 6-4, Long term history accumulation bandwidth: 9.7, 4.9, 2.4, 1.2, 0.61, 0.03 mHz Bits3-2, Short term history accumulation bandwidth: 2.5, 1.24, 0.62, 0.31 Hz Bits 1-0, Ramp control: none, 1, 1.5, 2 ppm/s
0x4e	T4_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode, 4 bits/reference
0x54	T4_PLL_Status	7-0	R	OOP, LOL, LOS, Sync, HHR, AHR, SAP
0x55	T4_Accu_Flush	0-0	W	0: Flush/reset the long-term history, 1: Flush/reset both the long-term and the device holdover history
0x56	CLK0_Sel	1-0	R/W	155.52/125 MHz clock select or disable for CLK0
0x57	CLK1_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or disable select for CLK1
0x58	CLK2_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or disable select for CLK2
0x59	CLK3_Sel	5-0	R/W	8kHz output 50% duty cycle or pulse width selection for CLK3
0x5a	CLK4_Sel	5-0	R/W	2kHz output 50% duty cycle or pulse width selection for CLK4
0x5b	CLK5_Sel	1-0	R/W	DS3/E3 select for CLK5
0x5c	CLK6_Sel	3-0	R/W	DS1 x n / E1 x n selector for CLK6
0x5d	CLK7_Sel	1-0	R/W	DS1/E1 selector for CLK7
0x5e	Intr_Event	9-0	R/W	Interrupt event
0x60	Intr_Enable	9-0	R/W	Interrupt enable
0x62	T0_MS_PHE	19-0	R	Round-trip phase delay of T0's cross-couple data links
0x65	CLK8_Sel	1-0	R/W	155.52/125 MHz clock select or disable for CLK8
Extra Registers if **LM** is configured as ***BUS_LOAD_MODE***				
0x70	Bus_Loader_Status	2-0	R	Status of the bus loader of the configuration data
0x71	Bus_Loader_Data	7-0	W	Data port of the bus loader of the configuration data
0x72	Bus_Loader_Counter	13-0	R	Data counter of the bus loader of the configuration data
Extra Registers if **LM** is configured as ***EEP_LOAD_MODE***				
0x70	EEP_Loader_Checksum	0-0	R	Checksum status of the EEPROM loader of the configuration data
0x71	EEP_Controller_Mode	7, 0	R/W	Mode of the EEPROM controller
0x72	EEP_Controller_Cmd	1-0	W	Command to the EEPROM controller
0x73	EEP_Controller_Page	7-0	W	Page number to the EEPROM controller
0x74	EEP_Controller_Data	7-0	R/W	Data port of the EEPROM controller

General Description

The STC5230 is an integrated single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. Its highly integrated design implements all of the necessary reference selection, monitoring, filtering, synthesis, and control functions. An external OCXO or TCXO at 20 MHz completes a system level solution (see Functional Block Diagram, Figure 1).

STC5230 comes with two timing generators, T0 and T4, to implement the essential functions of ***Synchronous Equipment Timing Source*** (SETS). Each timing generator could either be in external-timing or self-timing. In external timing, a timing generator may individually select one of the external reference inputs as its active reference of its individual Digital Phase-Locked Loop (DPLL). In self-timing, the clock outputs are just synthesized from the local oscillator (the external TCXO/OCXO). T0 provides 8 of the chip's 9 clock outputs while T4 provides one clock output. Additionally, both T0 and T4 provide a cross reference output for master/slave applications.

Each timing generator can individually operate in ***Freerun***, ***Synchronized***, and ***Holdover*** modes. In synchronized mode, the DPLL phase-locks to the selected external reference. Phase lock may be set as arbitrary or zero phase offset between the active reference and clock outputs. Each DPLL's loop bandwidth may be programmed individually to vary DPLL's filtering function. Oppositely, both freerun and holdover modes are self-timing. In freerun mode, the clock outputs are synthesized and calibrated from the local oscillator. In holdover mode, the clock outputs are synthesized with a given frequency offset. This frequency offset could either be a frequency history previously accumulated by STC5230, or a user supplied frequency offset. The stability of freerun and holdover is simply determined by the local oscillator.

Reference frequencies are auto-detected. Each reference input is continuously monitored for activity and frequency offset. The activity monitoring is implemented with a leaky bucket accumulator. A reference is desiganted as "qualified" if it is active and its frequency offset is within the programmed range for a pre-programmed time.

Active references may be selected manually or automatically, individually selectable for T0 and T4. In manual mode, the active reference is selected under application control, independant of it's qualification status.

In automatic mode, the active reference is selected according to revertivity status, and each reference's priority and qualification. Reference priorities are individually programmable. T0 and T4 each have their own priority tables. While a current active reference is qualified, revertivity determines whether a higher priority qualified reference should preempt the current active reference.

All reference switches are performed in a hitless manner. When references are switched, the device will minimize phase transitions in the output clocks. A frequency ramp control feature also ensures smooth frequency transitions in/out of both freerun and holdover mode.

Both timing generators, T0 and T4, support master/slave operation for ***redundant applications***. T0 sends both the phase and reference selection information to the other T0 on the paired STC5230 via the proprietary SyncLink^{TM} cross-couple data link. T4 provides only the phase information by sending out 8kHz signal via the cross-couple path. STC5230 is capable to trace and report T0's round-trip phase delay of the cross-couple data links.

The phase of slave's clock outputs can be programmed to adjust in 0.1ns step to compensate the propagation and re-transmission delay of the cross-couple path. This could minimize the phase hits to the downstream devices while doing the master/slave switches.

The device comes with a serial bus interface (SPI). The application could access to the STC5230's internal control and status registers via the bus interface.

STC5230 is also capable of ***field upgrading***. The initialization of registers and PLL detailed behavior is defined by the hardware and firmware configuration data. The configuration data may be provided by the internal ROM or externally. When externally sourced, the data may be pumped either over the bus interface, or from an optional external EEPROM.

Detailed Description

Chip Master Clock Input

The device operates with an external 20MHz OCXO or TCXO as its master clock, connected to the **MCLK** input, pin 99.

The freerun clock may be digitally calibrated from MCLK by writing an offset to the **Freerun_Cal** register, (0x0e/0f), from -102.4 to +102.3 ppm, in 0.1ppm steps, in two's complement form. (See **Register Descriptions** section for details regarding register references in this section.)

Operating Mode General Description

The STC5230 includes both a T0 and T4 timing generators. Each timing generator has its own DPLL.

In general, each timing generator could either be in external-timing or self-timing mode individually. In external-timing, a timing generator may select any of the external references as the active reference for the DPLL. The active reference can be either one of the 12 input reference clocks, or the reference from the **T(0/4)_XSYNC_IN** cross-couple links in slave mode. In addition, T4 may select the clock output of T0 as its active reference. In self-timing, the clock outputs are synthesized from the MCLK (the external TCXO/OCXO) with a certain calibration or a given frequency offset.

In master mode, the timing generators may each operates in the **Freerun**, **Synchronized**, or **Holdover** mode. Slave mode is analogous to the synchronized/master. Both are in external-timing. In synchronized/master mode, the phase relation between the reference and the clock outputs could be configured as arbitrary or aligned. User could also program DPLL's loop bandwidth to vary the noise transfer function. In slave mode, the clock outputs phase-align to the cross-reference. Unlike in master mode, the loop bandwidth is fixed (107 Hz) in slave mode.

Holdover mode is analogous to the freerun mode. Both are in self-timing. The clock outputs are synthesized from the local oscillator with a certain calibration or a given frequency offset. The stability in these two modes is simply determined by the local oscillator.

Operating Mode Details

STC5230 is designed to provide smooth clock outputs to the downstream devices, even under the change of operating mode or reference switch. Both the phase and frequency transition will be continuous. The transfer into the self-timing mode (freerun and holdover) is designed to be free of frequency bump. A frequency ramp control limits the rate of frequency change when transferring in and out of self-timing mode.

Freerun/Master Mode

The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are synthesized and may be calibrated from MCLK and have the stability of the external TCXO/OCXO. The calibration offset may be programmed by the application by writing to the **Freerun_Cal** register, (0x0e/0f). The calibration offset may be programmed from -102.4 to +102.3 ppm, in 0.1ppm steps.

On all transitions into freerun or back from freerun, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d).

Holdover/Master Mode

Holdover Mode is analogous to the freerun mode. The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are synthesized from MCLK with a given frequency offset, which is centered on the digitally calibrated freerun clock. The clock outputs will have the stability of the external TCXO/OCXO. The application may select the source of the frequency offset from either a device accumulated holdover history or a user supplied frequency offset by writing the "HO_Usage" bit of the **T(0/4)_Control_Mode** register (0x1c/0x39). If the bit is set to **Device Accumulated History Holdover Mode**, the DPLL will use the device accumulated device holdover history to synthesize the clock outputs. If the bit is set to **User Supplied History Mode**, the DPLL outputs are synthesized according to an application supplied frequency offset, as provided in the **T(0/4)_User_Accu_History** registers (0x2c/0x49). To facilitate the user's accumulation of a holdover history, the user may read the short-term history of the current clock outputs from the **T(0/4)_Short_Term_Accu_History** register (0x28-0x2b/0x45-0x48).

On all transitions into holdover or back from holdover, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d).

Synchronized/Master Mode

In synchronized mode, the DPLL phase-locks and track to the selected input reference. the timing generator is in external-timing. The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are all synchronized to the selected input reference.

In this mode, "Phase Align Mode" bit of the **T(0/4)_Control_Mode** registers (0x1c, 0x39) determines the output clock to input reference phase alignment mode. If the bit is set as **Arbitrary** mode, the DPLL will be in frequency locking stage initially. When the synchronization achieved, the clock output phase relationship relative to the reference input will be reset and locked (phase rebuild). If the bit is set as **Phase Align** mode, the output clocks are phase aligned to the selected reference. (It should be noted that output-to-reference phase alignment is meaningful only in those cases where the output frequency and reference are the same or related by an integer ratio.)

After reference switch or re-lock (due to loss of signal or loss of lock), the DPLL will be in pull-in process initially. If the phase mode is set to be arbitrary, the pull-in process will be frequency-locking only until a synchronization achieved. When a synchronization achieved, the clock output phase relationship relative to the reference input will be reset and locked. If the phase mode is set to be aligned, the pull-in process will be in phase-locking mode since the beginning. The pull-in process may prologue to 60+ seconds in normal situation.

The DPLL's loop bandwidth may be set independently. Loop bandwidth is programmable from 90mHz to 107Hz by writing to the **T(0/4)_Bandwidth** registers (0x1d/ 0x3a).

There are two special cases of the synchronized mode: **(a) Zombie mode** - If the signal of the active reference is lost, the DPLL output is generated according to the short-term history of the last moment; and **(b) Out of Pull-in Range mode** - If the selected reference exceeds the pull-in range as programmed by the application, the DPLL output may be programmed to stay at the pull-in range limit, or to follow the reference. This is programmed by writing to "OOP" bit of the **T(0/4)_Control_Mode** registers (0x1c/ 0x39), specifying whether to follow or not follow a reference that has exceeded the pull-in range. The frequency offset is centered by the digitally calibrated freerun clock.

Slave Mode

The slave mode is analogous to the synchronized/ master mode. The timing generators will enter this mode by bring the **T(0/4)_M/S** pin low. Different to the synchronized/master mode, the phase mode is to be aligned and the loop bandwidth is fixed to 107 Hz. The DPLL's clock outputs will follow the cross-reference no matter to the "OOP" bit of the **T(0/4)_Control_Mode** registers. The DPLL will lock and phase align on the **T0_XSYNC_IN** input and the 8kHz signal on the **T4_XSYNC_IN** input.

Operating Mode Transition Details

When the reference selection is set to manual mode, the operating mode could be selected by writing to the **T(0/4)_Manual_Active_Ref** registers (0x1f/0x3c). This could force the timing generator into freerun, synchronized, and holdover mode.

When the reference selection is set to automatic mode, the automatic reference selector not only picks up the active reference, but also decides the operating mode. The DPLL will enter synchronized mode if at least one reference is qualified and elected as the active reference. Otherwise, the operating mode will be either freerun mode or holdover mode, depending the existence of the holdover history.

Figure 2 shows the phase locked loop states and transitions for operation with automatic reference selection in Master mode. The transfer into and out of holdover mode is designed to be smooth and free of hits with frequency ramp control.

On all transitions into freerun or back from freerun, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d).

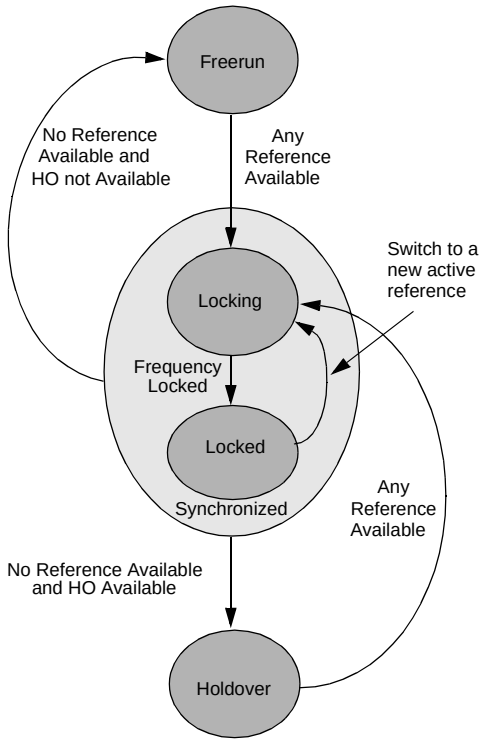


Figure 2: Operating mode transition in automatic reference selection (Master mode)

History Accumulation Details

Three holdover histories are built and maintained by each timing generator: the **short-term history**, the **long-term history**, and the **device holdover history**.

1. Short-Term History

This is a short-term average frequency of DPLL's clock outputs of all time. The weighted single-pole low-pass filter may be programmed for a -3dB point of 2.5, 1.24, 0.62, or 0.31 Hz by writing to the **T(0/4)_History_Ramp** register (0x30/0x4d). The short-term history is used in the zombie sub-mode. This history may be read from the **T(0/4)_Short_Term_Accu_History** registers (0x28-0x2b/0x45-0x48).

2. Long-Term History

This is a long-term average frequency of DPLL's clock outputs, while synchronized to a selected external reference. The weighted single-pole low-pass filter may be programmed for a -3dB point of 9.7, 4.9, 2.4, 1.2, 0.61, or 0.31 mHz by writing to the **T(0/4)_History_Ramp** register (0x30/0x4d). Internally, an express mode is used after reset by applying a lower time constant for the first 15 minutes to speed up the history accumulation process. This accumulation process will be reset whenever the selected reference is switched or loss of lock occurs. The accumulation process will then resume after the synchronization achieved - the assertion of "SYNC" bit in the **T(0/4)_DPLL_Status** register (0x37/0x54). Additionally, the application may flush/rebuild this long-term history by writing either "0" or "1" to the **T(0/4)_Accu_Flush** register (0x38/0x55). The long-term history may be read from the **T(0/4)_Long_Term_Accu_History** registers (0x24-0x27/0x41-0x44).

3. Device Holdover History

When the timing generator enters the holdover mode with the history usage programmed as Device Accumulated History Holdover Mode, this history determines the **CLK(0-6,8)** (**CLK7** for T4) clock outputs. The initial history will begin and continuously being updated by the long-term history after the 15 minute express mode time has completed. Updating will stop if the long term history accumulation process is reset as a result of a reference switch or loss of lock. Thus, the previous holdover history will persist until a new long term history is accumulated following a reference switch or the attendant re-building of the long term history after loss of lock. The "AHR" bit of the T(0/4)_DPLL_Status registers (0x37/0x54) is set to "1" during updating, but will revert to "0" when updating stops. Additionally, the application may reset this holdover history by writing "1" to the T(0/4)_Accu_Flush register (0x38/0x55).

Phase-Locked Loop Status Details

The **T(0/4)_PLL_Status** registers (0x37/0x54) contain the detailed status of DPLL, including the signal activity of the active reference, the synchronization status, and the availability of the holdover histories.

Applications can program the **Intr_Enable** register to enable/disable the interrupts (**pin EVENT_INTR**) trigged by the status change of **T(0/4)_PLL_Status** registers.

SYNC bit
In external-timing mode (e.g., slave and synchronized/master modes), this bit indicates the achievement of the synchronization. This bit won't be asserted in self-timing mode (e.g., freerun and holdover modes).

LOS bit
In external-timing mode (e.g., slave and synchronized/master modes), this bit indicates the loss of signal of the active reference. This bit won't be asserted in self-timing mode (e.g., freerun and holdover modes).

LOL bit
In external-timing mode (e.g., slave and synchronized/master modes), the DPLL will raise the event of loss of lock if it fails to achieve or maintain the lock to the active reference. This bit won't be asserted in self-timing mode (e.g., freerun and holdover modes). This bit is also not complemented to the SYNC bit. Both bits won't be asserted when the DPLL is still in the pull-in process.

OOP bit
This bit indicates the out of pull-in range of the active reference in external-timing mode (e.g., slave and synchronized/master modes). This bit won't be asserted in self-timing mode (e.g., freerun and holdover modes). The frequency offset is centered on the digitally calibrated freerun clock.

SAP bit
This bit indicates whether the DPLL's output clocks stop following the active reference because of the frequency offset of the active reference is out of pull-in range. The application can write to **T(0/4)_Control_Mode** register to program whether the DPLL shall follow the active reference out of the specified pull-in range.

AHR bit
This bit indicates whether the device holdover history is tracking on the current active reference (updating by the long-term history).

HHA bit
This bit indicates the availability of the holdover history, which could be either the user provided history or the device holdover history.

Reference Input Monitoring and Qualification

The STC5230 accepts 12 external reference inputs at 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, 50MHz, or 125MHz. Input frequencies are detected automatically. The autodetected frequency of any reference may be read by selecting the reference in the **Ref_Selector** register (0x15) and then reading the frequency from register **Ref_Frq_Offset** (0x17).

Each input is monitored and qualified for activity and frequency offset. Activity monitoring is accomplished with a leaky bucket accumulation algorithm, as shown in figure 3. The "leaky bucket" accumulator has a fill observation window that may be set from 1 to 16 ms, where any hit of signal abnormality (or multiple hits) during the window increments the bucket count by one. The leak observation window is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a consecutive, non-overlapping manner. The bucket accumulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

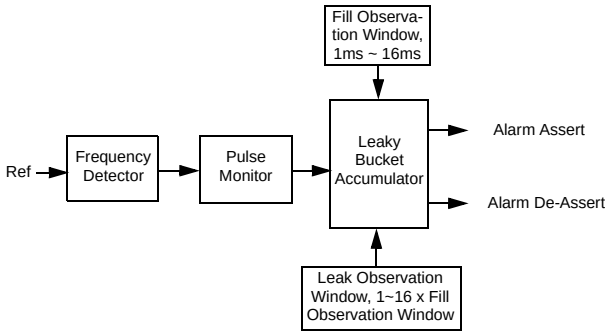


Figure 3: Activity Monitor

Applications can write to the following registers to configure the activity monitor: **Fill_Obs_Window** (0x09), **Leak_Obs_Window** (0x0a), **Bucket_Size** (0x0b), **Assert_Threshold** (0x0c), and **De_Assert_Threshold** (0x0d).

User can set the bucket size equal to 0 to turn off the activity monitor. This de-asserts the activity alarms of all the references. Otherwise, a non-zero bucket size must be greater than or equal to the alarm assert

threshold value, and the alarm assert threshold value must be greater than the alarm de-assert value. STC5230 will ignore the writing to these three registers if the value violates the rules. User shall carefully plan the scenario of activity monitor re-configuration.

Alarms appear in the **Refs_Activity** register (0x18,0x19). A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

Reference inputs are also monitored and qualified for frequency offset.

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification_Range** (0x12,0x13), and a disqualification range set up to 102.3 ppm, by writing to register **Disqualification_Range** (0x10,0x11). The qualification range must be set less than the disqualification range. Additionally, a qualification timer may be programmed from 0 to 63 seconds by writing to register **Qualification_Timer** (0x14). The pull-in range is the same as the disqualification range.

The frequency offset is centered at the digitally calibrated freerun clock. Each value of may be read by selecting the reference in the **Ref_Selector** register (0x15) and then reading the offset value from register **Ref_Frq_Offset** (0x16,0x17).

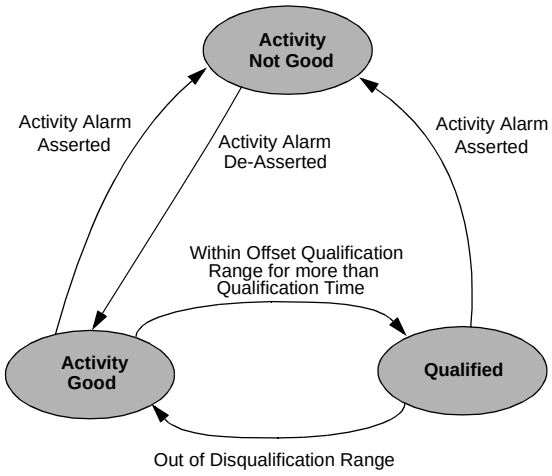


Figure 4: Reference Qualification Scheme

Figure 4 shows the reference qualification scheme. A reference is qualified if it has no activity alarm and is within the qualification range for more than the qualification time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if the activity alarm is off and the reference is within the qualification range for more than the qualification time.

The reference qualification status of each reference may then be read from register **Refs_Qual** (0x1a/1b).

Active Reference Selection

The T0 and T4 timing generators may be individually operated in either manual or automatic input reference selection mode. The mode is selected via the **T(0/4)_Control_Mode** registers (0x1c/0x39).

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference. This mode is selected via the **T(0/4)_Control_Mode** (0x1c/0x39) registers. The reference is selected by writing to the **T(0/4)_Manual_Active_Ref** (0x1f/0x3c) registers.

Automatic Reference Selection Mode

In automatic reference selection mode, the device will select one pre-qualified reference as the active reference. This mode is set via the **T(0/4)_Control_Mode** (0x1c/0x39) registers.

The active reference is picked according to its indicated priority in the reference priority table, registers **T(0/4)_Priority_Table** (0x31~0x36/0x4e~0x53). Each reference has one entry in the table, which may be set to a value from 0 to 15. '0' masks-out the reference, while 1 to 15 set the priority, where '1' has the highest, and '15' has the lowest priority. The highest priority pre-qualified reference then is a candidate to be the active reference. If multiple references share the same priority, the one who has be qualified with longer duration will win the tie-break.

This active reference candidate will be promoted to be active reference immediately if no active reference exists. The operating mode will then enter synchronized mode.

If the candidate reference is different to the existing active reference, this candidate may or may not revert

and pre-empt the existing active reference. This is determined by either enabling or disabling the "revertive" bit of the **T(0/4)_Control_Mode** (0x1c/0x39) to "1" for revertive or to "0" for non-revertive operation.

When reversion (pre-emption) is enabled, the candidate reference will be selected immediately as the new active reference. When reversion is disabled, the current active reference will not be pre-empted by any candidate until it is disqualified.

The automatically selected active reference for each DPLL may be read from **T(0/4)_Auto_Active_Ref** (0x1e/0x3b) registers.

The pre-qualification scheme is described in the **Reference Inputs Monitoring and Qualification** section.

Output Clocks

The clock output section includes 4 timing generators, an APLL, and four dividers, and generates eight synchronized clocks, as shown in figure 5.

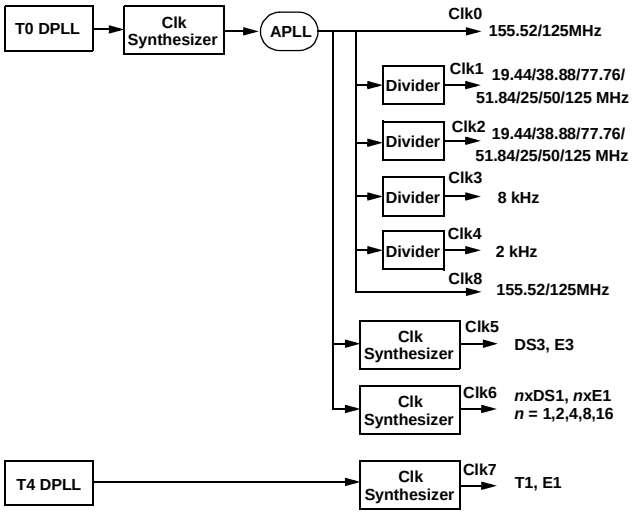


Figure 5: Output Clocks

The first synthesizer drives an analog PLL and generates six output clocks. It is driven from the T0 DPLL:

- **CLK0**: 155.52/125 MHz (LVPECL), selected or disabled by writing the **CLK0_Sel** register (0x56).
- **CLK1**: Programmable at 19.44MHz, 38.88MHz, 51.84MHz, 77.76 MHz, 25MHz, 50MHz, 125MHz, and disabled, by writing to the **CLK1_Sel** register (0x57).
- **CLK2**: Programmable at 19.44MHz, 38.88MHz, 51.84, 77.76 MHz, 25MHz, 50MHz, 125MHz, and disabled, by writing to the **CLK2_Sel** register (0x58).
- **CLK3**: 8kHz, 50% duty cycle or programmable pulse width, and may be disabled by writing to the **CLK3_Sel** register (0x59).
- **CLK4**: 2kHz, 50% duty cycle or programmable pulse width, and may be disabled by writing to the **CLK4_Sel** register (0x5a).
- **CLK8**: the second pair of 155.52/125 MHz (LVPECL), selected or disabled by writing the **CLK8_Sel** register (0x65).

Two more synthesizers generate additional clocks from the T0 DPLL:

- **CLK5**: Either DS3 or E3 rate, or "disabled", programmed by writing to the **CLK5_Sel** register (0x5b).
- **CLK6**: Programmable at nxDS1 or nxE1 rate, where n=1,2,4,8,16, or may be disabled, by writing to the **CLK6_Sel** register (0x5c).

One synthesizer is driven by the T4 DPLL:

- **CLK7**: Either DS1 or E1 rate, or "disabled", programmed by writing to the **CLK7_Sel** register (0x5d), bits 0 - 1.

When a clock output is disabled, the pin is tri-stated.

In addition, the **T0_XSYNC_OUT** output provides phase information and state data for master/slave operation of the T0 timing generators. The **T4_XSYNC_OUT** output provides an 8kHz signal for master/slave operation of the T4 timing generator.

Note that **CLK0,1, 2, 5, 6** and **8** are phase aligned with **CLK3** (8kHz) as shown in Figure 6. **CLk3** is phase aligned with **CLK4** (2kHz).

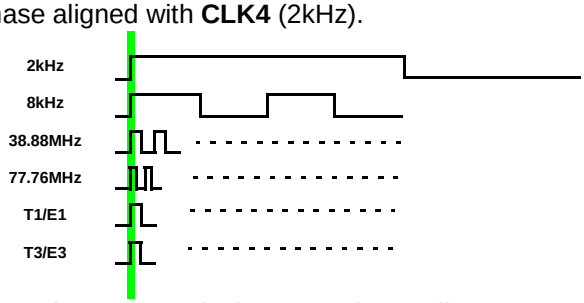


Figure 6: T0 clock output Phase Alignment

Master/Slave Configuration

Pairs of STC5230 devices may be operated in a master/slave configuration for added reliability, as shown in Figure 7.

Devices are configured as master/slave pair by cross-connecting their respective **T(0/4)_XSYNC_OUT** and/or **T(0/4)_XSYNC_IN** pins. The **T(0/4)_MS** pins determine the master or slave mode for each timing generator: 1=Master, 0=Slave. Thus, master/slave state is always manually controlled by the application. The slave T0 synchronizes and phase-aligns in the 2kHz domain according to data received over the **T0_XSYNC_OUT** / **T0_XSYNC_IN** data link from the paired partner. The slave T4 synchronizes and phase-aligns to the 8kHz received on the **T4_XSYNC_OUT** / **T4_XSYNC_IN** connection from the paired partner as well.

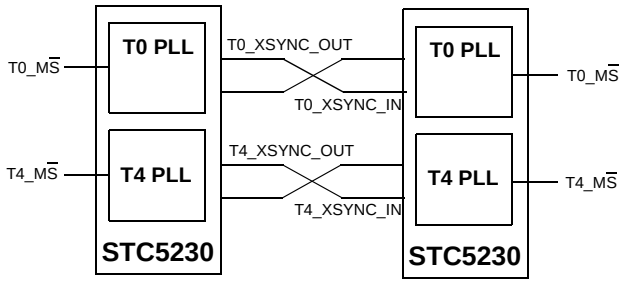


Figure 7: Master/Slave Pair

The T0 and T4 may be operated completely independent of each other – either or both may be cross-connected as master/slave pairs across two STC5230 devices, and master/slave states may be set the same or opposite within a given device.

When two STC5230 are wired in the master/slave pair configuration, the paired T0 timing generators can be running in master/master, master/slave, or slave/master modes. However, running in slave/slave mode will not be disable due to the clock resonance of the closed loop. Same applies to the paired T4 timing generators.

The **T0_T4_MS_Sts** register reflect the states of the **T(0/4)_MS** pins.

Master/Slave Operation

While in the slave configuration, the operation is analogous to the synchronized/master mode. The **T(0/4)_XSYNC_OUT** data link/8kHz signals provide the phase information of 2kHz (T0) and 8kHz (T4) for phase alignment between the master and the slave. In addition to phase information, **T0_XSYNC_OUT** also provides the reference selection state to ensure that later the new master may lock on the same reference if reference selection is in “automatic” mode.

Perfect phase alignment of the **Clk(x)** output clocks (between the paired timing generators in two devices) would require no delay on the cross-couple data link connection. To accommodate delay on the path, the STC5230 provides a programmable phase compensation feature. See figures 8 and 9. The slave’s **Clk(x)** outputs may be phase shifted from 0 to +409.5ns, in 100ps increments according to the contents of the **T(0/4)_Slave_Phase_Adj** (0x05/06, 0x07/08) registers to compensate for the path delay of the **T(0/4)_XSYNC_OUT** to **T(0/4)_XSYNC_IN** connections. This offset may therefore be programmed to exactly compensate for the actual path delay associated with the particular application's cross-couple traces. Thus, master/slave switches with the STC5230 devices may be accomplished with near-zero phase hits to the downstream devices.

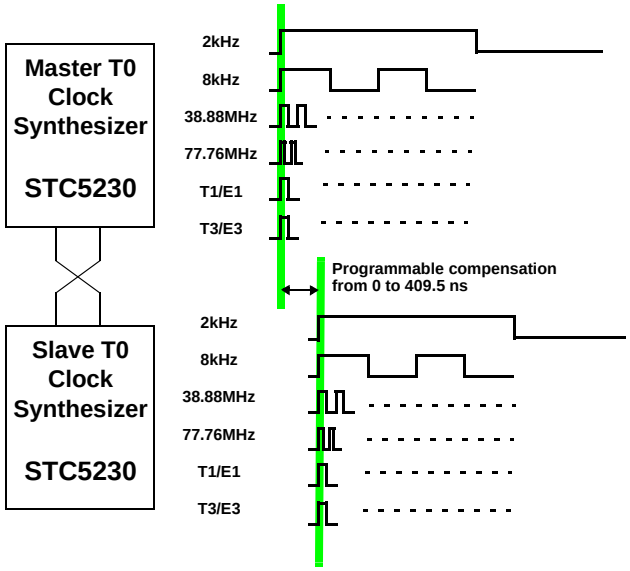


Figure 8: T0 **CLK0-6,8** Phase Alignment and Master/Slave skew Control

STC5230 is capable to trace and report the round-trip phase delay of T0’s cross-couple links. While T0 is configured as in master mode in redundant application, the phase delay between **T0_XSYNC_OUT** and

T0_XSYNC_IN pins is continously measured. User can obtain the phase delay by reading **T0_MS_PHE** register (0x62-0x64). Advanced users can use this information for their own further fault detection.

The first time a timing generator becomes a slave, such as immediately after power-up, its output clock phase starts out arbitrary, and will quickly phase-align to the master unit. The phase error will be eliminated (or converged to the programmed phase offset). The whole pull-in-and-lock process will complete in about 16 seconds. There is no frequency ramp protection in slave mode.

Activity of the signals on the **T(0/4)_XSYNC_IN** pins is available in the **Refs_Activity** register (0x18/19). (The leaky bucket algorithms are not applied to these signals.)

Note the phase alignment of all clock outputs from the T0 timing generator with the 2kHz output.

Once a pair of timing generators has been operating in aligned master/slave mode, and a master/slave switch occurs, the timing generator that becomes master will maintain its output clock phase and frequency while a phase rebuild is performed on its selected reference input. Therefore, as master mode operation commences, there will be no phase or frequency hits on the clock output. Assuming the phase offset is programmed for the actual delay of this cross-couple path, there will again be no phase hits on the output clock of the timing generator that has transitioned from master to slave.

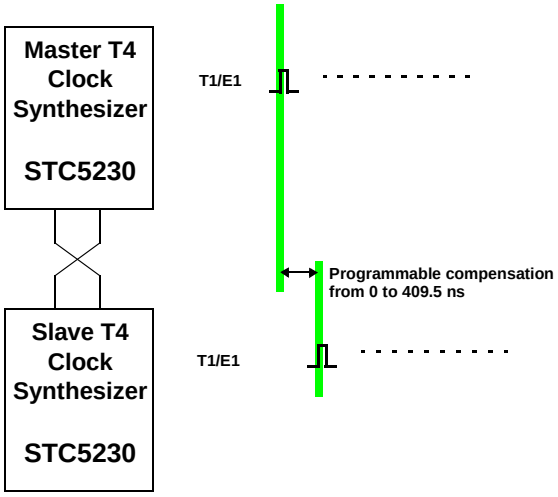


Figure 9: T4 **CLK7** Master/Slave Skew Control

Event Interrupts

STC5230 could provide notice interrupts to the host processor via pin EVENT_INTR (pin 32). A hand of certain events can be programmed to trig interrupts. User can turn on and off of each event individually by writing to register **Intr_Enable** (0x60-0x61). The associated events which trigged interrupts will be latched. After detected the assert of interrupt pin, application can read the list of latched events from register **Intr_Event** (0x5e-0x5f). User can clear the events by writing a '1' to the bit position of each related event. The pin **EVENT_INTR** returns to normal when no more event latched.

There are 10 different events can be programmed to trig the interrupts. The list covers the some status change of each timing generator and the change of qualification status of input references. The status change of the timing generator includes the change of the active reference in automatic reference selection mode, the change of the DPLL status, and the change of the cross reference activity. Each event could be enabled and disabled individually.

Field Upgrade Feature

The initialization of registers and DPLL detailed behavior is defined by the hardware and firmware configuration data. Following any device reset, either via power-up or operation of the reset pin, the device needs to be loaded with the configuration data. This data may be loaded from the internal ROM (programmed with factory default data), an optional external EEPROM, or from the bus interface.

Externally supplied data provides the option to accept future field upgrades. For external data loading, the manufacturer may provide the configuration data per a specific customer agreement.

Load mode configuration pins

The load mode configuration pins **LM0** and **LM1** determine the configuration data pump method, as shown in table 5:

Note that the Load Mode pins should not both be high, as device damage may occur.

In the ROM load mode, the configuration data is loaded from the internal ROM, which is loaded with the nominal manufacturer's data. Data loading occurs automatically on power up or after a reset.

Table 5: Load Mode Configuration Pins

LM1,LM0	Description
0,0	ROM load mode
0,1	Bus load mode
1,0	EEPROM load mode
1,1	Reserved - do not use

Table 6: Compatible EEPROMs

Manufacturer	Part Number
ATMEL	AT25128A

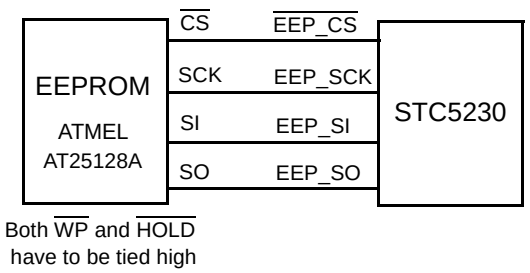


Figure 10: EEPROM Configuration

In the bus load mode, the configuration data is loaded from the SPI bus interface by the application, using the device bus load register interface. Data is provided to the customer per an agreement with the manufacturer. The load procedure is described in the following section.

In the EEPROM load mode, an EEPROM loader will load the configuration data from an optional external EEPROM. Data will be provided by the manufacturer per an agreement with the customer. The configuration data may be read from or write to the external EEPROM via the SPI bus interface.

When the EEPROM load mode is selected, data loading occurs automatically immediately following a power up or reset. The EEPROM interface is shown in Figure 10.

Bus Load Process

Data loading via the bus mode is accomplished using the **Bus_Loader_Status** (0x70), **Bus_Loader_Data** (0x71), and **Bus_Loader_Counter** (0x72) registers. User shall follow the procedure below:

```
/* --- *
The data array data[10496] contains the hardware/firmware
configuration data, starting from index 0.
 * --- */

Procedure Bus_Load
begin

    Label_Repeat:

  - busy wait until bit "bus ready" in the
    Bus_Loader_Status is equal to '1';
  - for i: = 0 to 10,495 step 1
    begin
      - write data[i] to register Bus_Loader_Data;
      - busy wait until bit "bus ready" in register
        Bus_Loader_Status is equal to '1';
    end

  - if bit "load complete" in register Bus_Loader_Status is
    equal to '0'
    begin
      /* loading failed */
      - reset this device by asserting pin RESET;
      - goto Label_Repeat;
    end

  - if bit "checksum status" in register
    Bus_Loader_Status is equal to '0'
    begin
      /* loading failed */
      - reset this device by asserting pin RESET;
      - goto Label_Repeat;
    end

    /* Bus Loading Success */

end of procedure Bus Load
```

The device will assert "load complete" bit in register **Bus_Loader_Status** after the application writes 10,496 bytes into register **Bus_Loader_Data**.

After the bit "load complete" is asserted, application shall read and check the bit "checksum status" of register **Bus_Load_Status**. "1" indicates the checksum passed; "0" indicates the failure of loading. CRC-16

checksum encryption is used in the configuration data to assure the detection of transmission error.

Should the load fail, the application must reset the device and repeat the load process.

Before the "bus ready" bit is asserted or after the "load complete" bit in register **Bus_Loader_Status** is asserted, all writes to the **Bus_Loader_Data** register will be ignored.

At any time in the process, the application may read the number of bytes that have been written from the **Bus_Loader_Counter** register.

EEPROM Load Process

When **LM** is configured as **EEP_LOAD_MODE**, the configuration data will be loaded from the optional external EEPROM by device's build-in EEPROM loader automatically. Application shall read and check the register EEP_CHECKSUM which indicates the CRC-16 checksum status of the loading process. If the download failed, the application must reset the device and repeat the check of this status again.

EEPROM: Read and Write

Application has to pump the configuration data into the external EEPROM before the normal operation if expecting to configure to load the data from EEPROM.

When **LM** is configured as **EEP_LOAD_MODE**, the application may read and write the configuration data from/to the external EEPROM via device's EEPROM controller using the register **EEP_Controller_Mode**, **EEP_Controller_Cmd**, **EEP_Controller_Page**, and **EEP_Controller_Data (0x71 to 0x74)**.

After pump (writing) the whole configuration data into the external EEPROM, application has to read it back and do the comparison to ensure no transmission error happened. The writing and reading procedures are as follows:

*Procedure **EEP_Write***
begin
/ --- **
*The data array **data**[10496] contains the hardware/ firmware configuration data, starting from index 0.*
*** --- */*
- *busy wait until bit "**ready**" in register **EEP_Controller_Mode** is equal to '1';*
- *write 0x01 to register **EEP_Controller_Mode;** /* turn on the write feature */*
- *write 0x00 to register **EEP_Controller_Cmd;** /* reset the page FIFO buffer */*
- *for i = 0 to 163 step 1*
  begin
  - *write **(i)** to register **EEP_Controller_Page;** /* set the page index */*
  - *for j = 0 to 63 step 1*
    begin
    - *write **data**[64*i+j] to register **EEP_Controller_Data;***
    end
  - *write 0x01 to register **EEP_Controller_Cmd;** /* issue the write command */*
  - *busy wait until bit "**ready**" in register **EEP_Controller_Mode** is equal to '1';*

  end
- *write 0x00 to register **EEP_Controller_Mode**; /* turn off the write feature */*

end of procedure EEP_Write

*Procedure **EEP_Read***
begin
- *busy wait until bit "**ready**" in register **EEP_Controller_Mode** is equal to '1';*
- *for i = 0 to 163 step 1*
  begin
  - *write **(i)** to register **EEP_Controller_Page;** /* set the page index */*
  - *write 0x02 to register **EEP_Controller_Cmd;** /* issue the read command */*
  - *busy wait until bit "**ready**" in register **EEP_Controller_Mode** is equal to '1';*
  - *for j = 0 to 63 step 1*
    begin
    - *read and copy the value of register **EEP_Controller_Data** into **data**[64*i+j];*
    end

  end

  / --- **
  *The data array **data**[10496] is then carrying the hardware/firmware configuration data, starting from index 0.*
  *** --- */*

end of procedure EEP_Read

Processor Interface Descriptions

The STC5230 supports the serial SPI bus interface. The description of SPI bus's interface timing is following:

The SPI interface bus mode uses the $\overline{\text{BUS\_CS}}$, BUS_ALE, BUS_RDB, and BUS_RDY pins, corresponding to CS, SCLK, SDI, and SDO respectively, with timing as shown in figures 11 and 12:

Serial Bus Timing

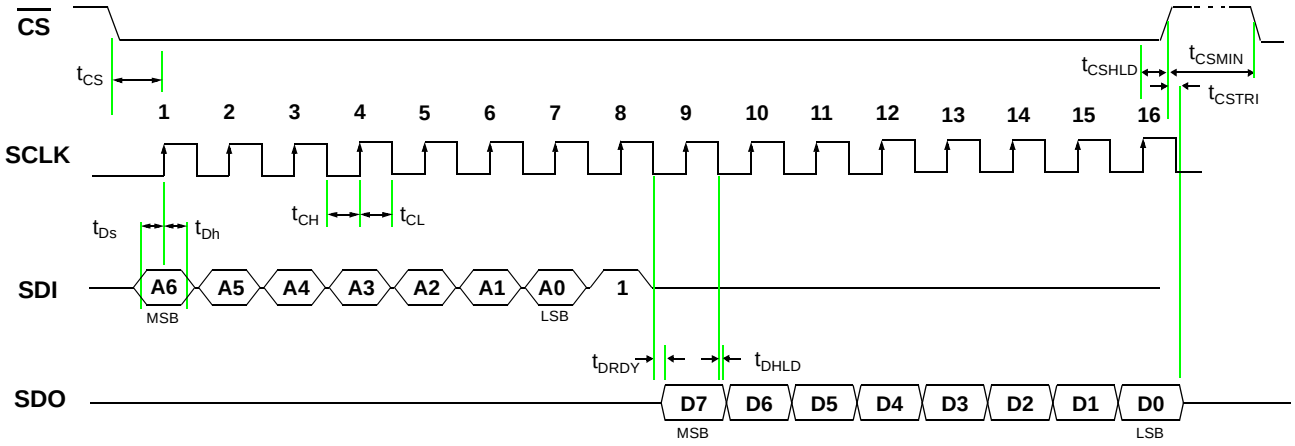


Figure 11: Serial Bus Timing, Read access

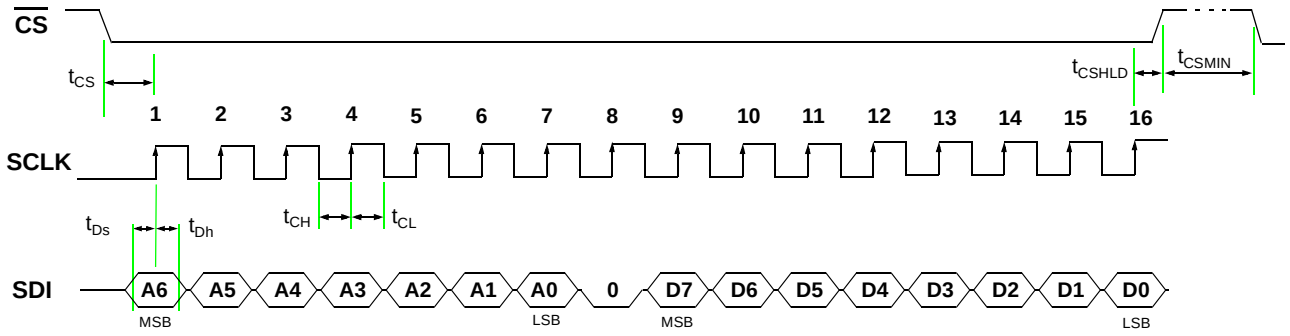


Figure 12: Serial Bus Timing, Write access

Table 7: Serial Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low to SCLK high	10		ns
t_{CH}	SCLK high time	25		ns
t_{CL}	SCLK low time	25		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Register Descriptions and Operation

General Register Operation

The STC5230 device has 1, 2, 3, and 4 byte registers. One-byte registers are read and written directly. Multiple -byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multibyte register read must commence with a read of the least significant byte first. This triggers a transfer of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multibyte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/ writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Clearing bits in the Interrupt Status Register

Interrupt event register (**Intr_Event**, 0x5e~0x5f) bits are cleared by writing a “1” to the bit position to be cleared. Interrupt bit positions to be left as is are written with a “0”.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x30							
0x01	0x52							

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

T0_T4_MS_Sts, 0x04 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Not used						T4 M/S	T0 M/S

Reflects the states of the **T0/T4_MASTER_SLAVE** select pins. 1 = Master, 0 = slave

T0_Slave_Phase_Adj, 0x05 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, lower 8 bits							
0x06	Not used				Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, upper 4 bits			

The T0 slave phase may be adjusted 0 to 409.5 ns relative to the cross couple input with 0.1 ns resolution. This is a 12 bit register, split across address 0x05 and 0x06.
Default value: 0

T4_Slave_Phase_Adj, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, lower 8 bits							
0x08	Not used				Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, upper 4 bits			

The T4 slave phase may be adjusted 0 to 409.5 ns relative to the cross couple input with 0.1 ns resolution. This is a 12 bit register, split across address 0x07 and 0x08.
Default value: 0

Fill_Obs_Window, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used				Leaky bucket fill observation window, m = 0 ~ 15			

Sets the fill observation window size for the reference activity monitor to (m+1) ms. The window size can be set from 1ms to 16ms.
Default value: m = 0, (1ms)

Leak_Obs_Window, 0x0a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0a	Not used				Leaky bucket fill observation window, n = 0 ~ 15			

Sets the leak observation window size for the reference activity monitor to (n + 1) times the fill observation window size.
Default value: n = 3, (4 times)

Bucket_Size, 0x0b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0b	Not used		Leaky bucket size, 0 ~ 63					

Sets the leaky bucket size for the reference activity monitor. Bucket size equal to 0 will set the leaky bucket active monitor off, which will not assert activity alarm. Otherwise, the bucket size must be greater than or equal to the alarm assert value. Invalid values will not be written to the register.

Default value: 20

Assert_Threshold, 0x0c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0c	Not used		Leaky bucket alarm assert threshold, 1 ~ 63					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Invalid values will not be written to the register.
Default value: 15

De_Assert_Threshold, 0x0d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0d	Not used		Leaky bucket alarm de-assert threshold, 0 ~ 62					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Invalid values will not be written to the register.
Default value: 10

Freerun_Cal, 0x0e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0e	Lower 8 bits							
0x0f	Not used					Upper 3 bits		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, two's complement.
Default value: 0

Disqualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits							
0x11	Not used						Upper 2 bits	

Reference disqualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See the **Reference Input Monitoring and Qualification** section)
Default value: 110 (range = 11.0 ppm).

Qualification_Range, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Lower 8 bits							
0x13	Not used						Upper 2 bits	

Reference qualification range, from 0 to +102.3 ppm, in 0.1 ppm steps.
Default value: 100 (range = 10.0 ppm).

Qualification_Timer, 0x14 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Not used		0 ~ 63 s					

Reference qualification timer, from 0 to 63 s.
Default value: 10

Ref_Selector, 0x15 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	Not used				1 ~ 12 (0x1 ~ 0xc)			

Determines which reference data is displayed in register 0x16 and 0x17. Valid values from 1 to 12. Invalid values will not be written to the register.
Default value: 1

Ref_Frq_Offset, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Lower 8 bits of frequency offset							
0x17	Reference frequency				Upper 4 bits of frequency offset			

Displays the frequency offset and reference frequency for the reference selected by the **Ref_Selector** (0x15) register. Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun, in 0.1 ppm steps, two's complement. A value of -2048 indicates the reference is out of range.

The reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined):

0x17, bits 7 ~ 4	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz
4	2.048 MHz
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	125 MHz
14	Unknown
15	Reserved

Refs_Activity, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x19	Not used		T4_XSYNC_IN	T0_XSYNC_IN	Ref 12	Ref 11	Ref 10	Ref 9

Reference activity indicator, 0 = no activity, 1 = activity.

Refs_Qual, 0x1a (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1a	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x1b	Not used				Ref 12	Ref 11	Ref 10	Ref 9

Reference qualification indicator, 0 = not qualified, 1 = qualified.

T0_Control_Mode, 0x1c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1c	Not used		OOP: Out of Pull-in range: 0=Follow 1=Don't follow	Manual/ Auto 0=Manual 1=Auto	Revertive 0=Non-revertive 1=Revertive	HO_Usage 0=DHH 1=User	Not used	Phase Align Mode 0=Arbitrary 1=Align

Mode control bits for T0.

Phase Align Mode 0 = Arbitrary (use initial phase), 1 = Phase align
HO_Usage 0 = Device Holdover History (DHH) is used; 1 = User supplied history is used.
OOP In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range** (0x10). OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T0_Bandwidth, 0x1d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1d	Not used			Bandwidth select				

Sets the T0 loop bandwidth:

0x1d, bits 4 ~ 0	Bandwidth, Hz
0	107
1	50
2	24
3	12
4	5.9
5	2.9

0x1d, bits 4 ~ 0	Bandwidth, Hz
6	1.5
7	.73
8	0.37
9	0.18
10	0.09
31 ~ 11	Reserved

Default value: 6

T0_Auto_Active_Ref, 0x1e (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1e	Not used				Selection			

Indicates the automatically selected active reference for T0, when this T0 is a “master”. When this T0 is a “slave”, the master’s active reference is indicated. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T0_Manual_Active_Ref, 0x1f (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1f	Not used				Selection			

Selects the active reference for T0 in manual reference select mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

Default value: 0

T0_Device_Holdover_History, 0x20 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Bits 0 - 7 of 32 bit Device Holdover History							
0x21	Bits 8 - 15 of 32 bit Device Holdover History							
0x22	Bits 16 - 23 of 32 bit Device Holdover History							
0x23	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T0 relative to MCLK. 2’s complement. Resolution is 0.745×10^{-3}ppb.
Default value: 0

T0_Long_Term_Accu_History, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Bits 0 - 7 of 32 bit Long Term History							
0x25	Bits 8 - 15 of 32 bit Long Term History							
0x26	Bits 16 - 23 of 32 bit Long Term History							
0x27	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_Short_Term_Accu_History, 0x28 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x28	Bits 0 - 7 of 32 bit Short Term History							
0x29	Bits 8 - 15 of 32 bit Short Term History							
0x2a	Bits 16 - 23 of 32 bit Short Term History							
0x2b	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_User_Accu_History, 0x2c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2c	Bits 0 - 7 of 32 bit User Holdover History							
0x2d	Bits 8 - 15 of 32 bit User Holdover History							
0x2e	Bits 16 - 23 of 32 bit User Holdover History							
0x2f	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.
Default value: 0

T0_History_Ramp, 0x30 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	Not used	Long Term History Bandwidth			Short Term History Band-width		Ramp control	

Holdover bandwidth and ramp controls for T0:

0x30, bits 6 ~ 4	Long Term History -3dB Bandwidth
000	9.7 mHz
001	4.9 mHz
010	2.4 mHz
011	1.2 mHz
100	0.61 mHz
101	0.30 mHz

0x30, bits 3 ~ 2	Short Term History -3dB Bandwidth
00	2.5 Hz
01	1.24 Hz
10	0.62 Hz
11	0.31 Hz

0x30, bits 1 ~ 0	Ramp control
00	No Control
01	1 ppm/s
10	1.5 ppm/s
11	2 ppm/s

Default value: 0x27 (2.4mHz; 1.24Hz; 2ppm/s)

T0_Priority_Table, 0x31 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	Ref 2 Priority				Ref 1 Priority			
0x32	Ref 4 Priority				Ref 3 Priority			
0x33	Ref 6 Priority				Ref 5 Priority			
0x34	Ref 8 Priority				Ref 7 Priority			
0x35	Ref 10 Priority				Ref 9 Priority			
0x36	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x31 - 0x36, 4 bits	Reference Priority
0000	Disable reference
0001 ~ 1111	1 ~ 15

Default value: 0

T0_PLL_Status, 0x37 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x37	HHA 1=Available 0=Not available	AHR 1=Ready 0=Not ready	Reserved	SAP 1=Stop at pull-in range 0=Follow-ing	OOP 1=Out of pull-in range 0=In range	LOL 0=No LOL 1=LOL	LOS 0=No LOS 1=LOS	SYNC: 0=No Sync 1=Sync

SYNC Indicates synchronization has been achieved
LOS Loss of signal of the active reference
LOL Loss of lock (Failure to achieve or maintain lock)
OOP Out of pull-in range

AHR Active Holdover History Ready
HHA Holdover History Available
SAP Indicates the output clocks stop following the selected reference, caused by out of pull-in range

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T0_Accu_Flush, 0x38 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x38	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit zero determines which histories are flushed. Bit 0 = 0, Flush and reset T0 long term history only; bit 0 = 1, flush/reset both T0 long term history and the T0 device holdover history.

T4_Control_Mode, 0x39 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x39	Not used		OOP: Out of Pull-in range: 0=Follow 1=Don't follow	Manual/ Auto 0=Manual 1=Auto	Revertive 0=Non-revertive 1=Revertive	HO_Usage 0=DHH 1=User	Not used	Phase Align Mode 0=Arbitrary 1=Align

Mode control bits for T4.

Phase Align Mode 0 = Arbitrary (use initial phase), 1 = Phase align
HO_Usage 0 = Device Holdover History (DHH) is used; 1 = User supplied history is used.
OOP In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range** (0x10). OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T4_Bandwidth, 0x3a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3a	Not used			Bandwidth select				

Sets the T4 loop bandwidth:

0x3a, bits 4 ~ 0	Bandwidth, Hz
0	107
1	50

0x3a, bits 4 ~ 0	Bandwidth, Hz
2	24
3	12
4	5.9
5	2.9
6	1.5
7	.73
8	0.37
9	0.18
10	0.09
31 ~ 11	Reserved

Default value: 0

T4_Auto_Active_Ref, 0x3b (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3b	Not used				Selection			

Indicates the automatically selected active reference for T4. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T4_Manual_Active_Ref, 0x3c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3c	Not used				Selection			

Selects the active reference for T4 in manual reference select mode. Default value: 0

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14	Reserved
15	Lock on T0 output

T4_Device_Holdover_History, 0x3d (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3d	Bits 0 - 7 of 32 bit Device Holdover History							
0x3e	Bits 8 - 15 of 32 bit Device Holdover History							
0x3f	Bits 16 - 23 of 32 bit Device Holdover History							
0x40	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3}ppb.
Default value: 0

T4_Long_Term_Accu_History, 0x41 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x41	Bits 0 - 7 of 32 bit Long Term History							
0x42	Bits 8 - 15 of 32 bit Long Term History							
0x43	Bits 16 - 23 of 32 bit Long Term History							
0x44	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_Short_Term_Accu_History, 0x45 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x45	Bits 0 - 7 of 32 bit Short Term History							
0x46	Bits 8 - 15 of 32 bit Short Term History							
0x47	Bits 16 - 23 of 32 bit Short Term History							
0x48	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_User_Accu_History, 0x49 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x49	Bits 0 - 7 of 32 bit User Holdover History							
0x4a	Bits 8 - 15 of 32 bit User Holdover History							
0x4b	Bits 16 - 23 of 32 bit User Holdover History							
0x4c	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.
Default value: 0.

T4_History_Ramp, 0x4d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4d	Not used	Long Term History bandwidth			Short Term History band-width		Ramp control	

Holdover bandwidth and ramp controls for T4:

0x4d, bits 6 ~ 4	Long Term History -3dB Bandwidth
000	9.7 mHz
001	4.9 mHz
010	2.4 mHz

0x4d, bits 6 ~ 4	Long Term History -3dB Bandwidth
011	1.2 mHz
100	0.61 mHz
101	0.30 mHz

0x4d, bits 3 ~ 2	Short Term History -3dB Bandwidth
00	2.5 Hz
01	1.24 Hz
10	0.62 Hz
11	0.31 Hz

0x4d, bits 1 ~ 0	Ramp control
00	No Control
01	1 ppm/s
10	1.5 ppm/s
11	2 ppm/s

Default value: 0x27 (2.4mHz; 1.24Hz; 2ppm/s)

T4_Priority_Table, 0x4e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4e	Ref 2 Priority				Ref 1 Priority			
0x4f	Ref 4 Priority				Ref 3 Priority			
0x50	Ref 6 Priority				Ref 5 Priority			
0x51	Ref 8 Priority				Ref 7 Priority			
0x52	Ref 10 Priority				Ref 9 Priority			
0x53	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x4e - 0x53, 4 bits	Reference Priority
0000	Disable reference
0001 ~ 1111	1 ~ 15

Default value: 0

T4_PLL_Status, 0x54 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	HHA 1=Available 0=Not available	AHR 1=Ready 0=Not ready	Reserved	SAP 1=Stop at pull-in range 0=Follow-ing	OOP 1=Out of pull-in range 0=In range	LOL 0=No LOL 1=LOL	LOS 0=No LOS 1=LOS	SYNC: 0=No Sync 1=Sync

SYNC	Indicates synchronization has been achieved
LOS	Loss of signal of the active reference
LOL	Loss of lock (Failure to achieve or maintain lock)
OOP	Out of pull-in range
AHR	Active Holdover History Ready
HHA	Holdover History Available
SAP	Indicates the output clocks stop following the selected reference, caused by out of pull-in range

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T4_Accu_Flush, 0x55 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x55	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit zero determines which histories are flushed. Bit 0 = 0, Flush and reset T4 long term history only; bit 0 = 1, flush/reset both T4 long term history and the T4 device holdover history.

CLK0_Sel, 0x56 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	Not used						CLK0 Select	

Selects or disables the CLK0 output.
Default value: 0

0x56, bits 1 ~ 0	CLK0 output
0	Disabled
1	155.52MHz
2	125MHz
3	Reserved

CLK1_Sel, 0x57 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	Not used					CLK1 Select		

Selects or disables the CLK1 output.

0x57, bits 2 ~ 0	CLK1 output
0	Disabled
1	19.44MHz

0x57, bits 2 ~ 0	CLK1 output
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 1

CLK2_Sel, 0x58 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x58	Not used					CLK2 Select		

Selects or disables the CLK2 output.

0x58, bits 1 ~ 0	CLK2 output
0	Disabled
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 2

CLK3_Sel, 0x59 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59	Not used		CLK3 Select					

Selects or disables the CLK3 output, and sets the pulse width. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x59, bits 5 ~ 0	CLK3 8kHz output
0	Disabled
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK4_Sel, 0x5a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5a	Not used		CLK4 Select					

Selects or disables the CLK4 output, and sets the pulse width. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x5a, bits 5 ~ 0	CLK4 2kHz output
0	Disabled
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK5_Sel, 0x5b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5b	Not used						CLK5 Select	

Selects or disables the CLK5 output.

0x5b, bits 1 ~ 0	CLK5 output
0	Disabled
1	44.736MHz (DS3)
2	34.368MHz (E3)
3	Reserved

Default value: 2

CLK6_Sel, 0x5c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5c	Not used				CLK6 Select			

Selects or disables the CLK6 output.

0x5c, bits 3 ~ 0	CLK6 output
0	Disabled
1	2.048MHz
2	4.096MHz
3	8.192MHz
4	16.384MHz
5	32.768MHz
6, 7, 8	Reserved
9	1.544MHz
10	3.088MHz
11	6.176MHz
12	12.352MHz
13	24.704MHz
14, 15	Reserved

Default value: 1

CLK7_Sel, 0x5d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5d	Not used						CLK7 Select	

Selects or disables the CLK7 output.

0x5d, bits 1 ~ 0	CLK7 output
0	Disabled
1	1.544MHz (T1)
2	2.048MHz (E1)
3	Reserved

Default value: 2

Intr_Event, 0x5e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5e	Event 7: T4 cross reference changed from non-active to active	Event 6: T4 cross reference changed from active to non-active	Event 5: T4 DPLL status changed	Event 4: T4 active reference changed in auto selection mode	Event 3: T0 cross reference changed from non-active to active	Event 2: T0 cross reference changed from active to non-active	Event 1: T0 DPLL status changed	Event 0: T0 active reference changed in auto selection mode
0x5f							Event 9: Any reference changed from disqualified to qualified	Event 8: Any reference changed from qualified to disqualified

Interrupt event, 0 = no event, 1 = event occurred. Interrupt 8 and 9 apply to the 12 reference inputs only. Interrupts are cleared by writing “1’s” to the bit positions to be cleared (See **General Register Operation, Clearing bits in the Interrupt Status Register** section).

Intr_Enable, 0x60 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	Intr 7 Enable	Intr 6 Enable	Intr 5 Enable	Intr 4 Enable	Intr 3 Enable	Intr 2 Enable	Intr 1 Enable	Intr 0 Enable
0x61							Intr 9 Enable	Intr 8 Enable

Interrupt disable/enable, 0 = disable, 1 = enable.
Default value: 0

T0_MS_PHE, 0x62 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x62	Bits 0 - 7 of 20 bit Phase Delay							
0x63	Bits 8 - 15 of 20 bit Phase Delay							
0x64	Not used				Bits 16 - 19 of 20 bit Phase Delay			

T0's phase delay of the round-trip cross-couple links from the master to the slave then back to the master. 2's complement. Resolution is (12.5ns/64 ~= 0.2ns). Range from (-125us/2) to (+125us/2). This value is valid only when T0 is configured as in master mode.

CLK8_Sel, 0x65 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x65	Not used						CLK8 Select	

Selects or disables the CLK8 output.
Default value: 0

0x65, bits 1 ~ 0	CLK8 output
0	Disabled
1	155.52MHz
2	125MHz
3	Reserved

Bus_Loader_Status, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Not used					load complete	bus ready	Checksum status

If bus load data mode has been selected with pins **LM0,1**, this register Indicates the loader's status.

load complete Set to 1 when the loading process is complete in the bus load mode.
bus ready Set to 1 when the device is ready to load data in the bus load mode.
checksum status Set to 1 if the data load is successful (CRC-16 checksum over the 10,496 bytes of configuration data passes) in the bus load data mode. The "checksum status" bit is valid only after the "load complete" bit has been set.

Bus_Loader_Data, 0x71 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Data							

If bus load data mode has been selected with pins **LM0,1**, the hardware and firmware configuration data is written to this register.

Bus_Loader_Counter, 0x72 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Bits 0 -7							
0x73	Not used		Bits 8 - 13					

If bus load data mode has been selected with pins **LM0,1**, this register indicates the number of bytes that have been written to the **Bus_Loader_Data** register.

EEP_Loader_Checksum, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Not used							Checksum status

If EEPROM load data mode has been selected with pins **LM0,1**, this register indicates the checksum status of the loading process from the external EEPROM.

checksum status Set to 1 if the data load is successful (ensured by the CRC-16 checksum encryption over the 10,496 bytes of configuration data) in the EEPROM load data mode.

EEP_Controller_Mode, 0x71 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	ready	no used						writable

If EEPROM load data mode has been selected with pins **LM0,1**, this register indicates the readiness of the EEPROM controller and can be used to turn on and off the writing feature to the external EEPROM.

ready Set to 1 when the controller's page FIFO buffer is ready to be used for further read and write data from/to the external EEPROM.

writable This bit is used to enable/disable the writing feature to the external EEPROM. Write '1' to this bit makes the EEROM writable. Writing '0' to this bit makes the EEPROM not writable.

EEP_Controller_Cmd, 0x72 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	no used						command	

If EEPROM load data mode has been selected with pins **LM0,1**, this register is used to issue the reset, write, and read command to the EEPROM controller.

command=0 reset and clean up the page FIFO buffer.

command=1 trig the EEPROM controller to write the contents in the 64-byte page FIFO buffer to a certain page of the external EEPROM.

command=2 trig the EEPROM controller to read and copy the 64-byte content of certain page of the external EEPROM into the page FIFO buffer.

command=3 reserved

EEP_Controller_Page, 0x73 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x73	Page number							

If EEPROM load data mode has been selected with pins **LM0,1**, this register is used to specify the index of the page of the EEPROM for the further read and write command. The valid value is from 0 to 163.

EEP_Controller_Data, 0x74 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x74	data							

If EEPROM load data mode has been selected with pins **LM0,1**, the data is read and written from/to the page FIFO buffer via this register.

Noise Transfer Functions

User may write to T(0/4)_Bandwidth registers to set the loop bandwidth of the DPLL of each timing generator. The noise transfer function of the filtering of the DPLL is decided by the loop bandwidth. The figure 13 shows the noise transfer functions as the loop bandwidths varying from 90mHz to 107Hz.

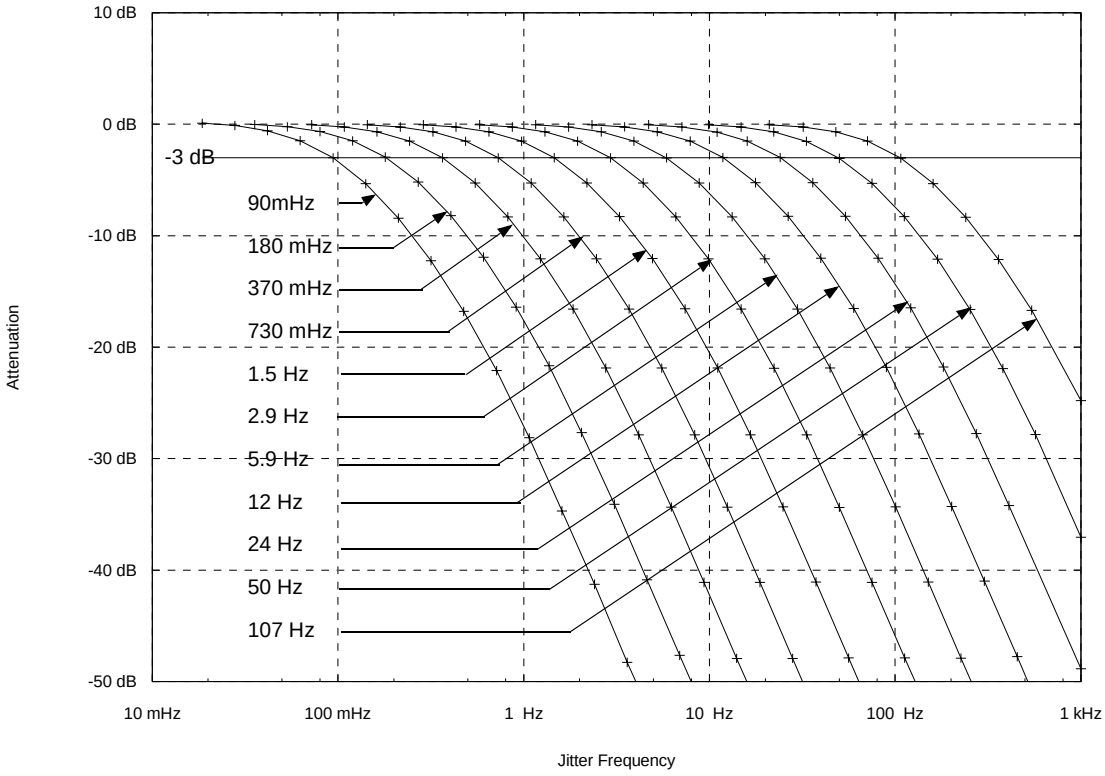


Figure 13: Noise Transfer Functions

Application Notes

This section describes typical application use of the STC5230 device. The General section applies to all application variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3 and 1.8V digital power and 1.8V analog power input. All digital I/O is at 3.3V, LVTTL compatible, except of the two pairs of LVPECL clock outputs.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints. On power-up, it is desirable to have the 3.3V either lead or be coincident with, but not lag the application of both 1.8V supplies.

Digital ground should be provided by as continuous a ground plane as possible. A separated analog ground plane is recommended.

Note: Un-used reference inputs must be grounded.

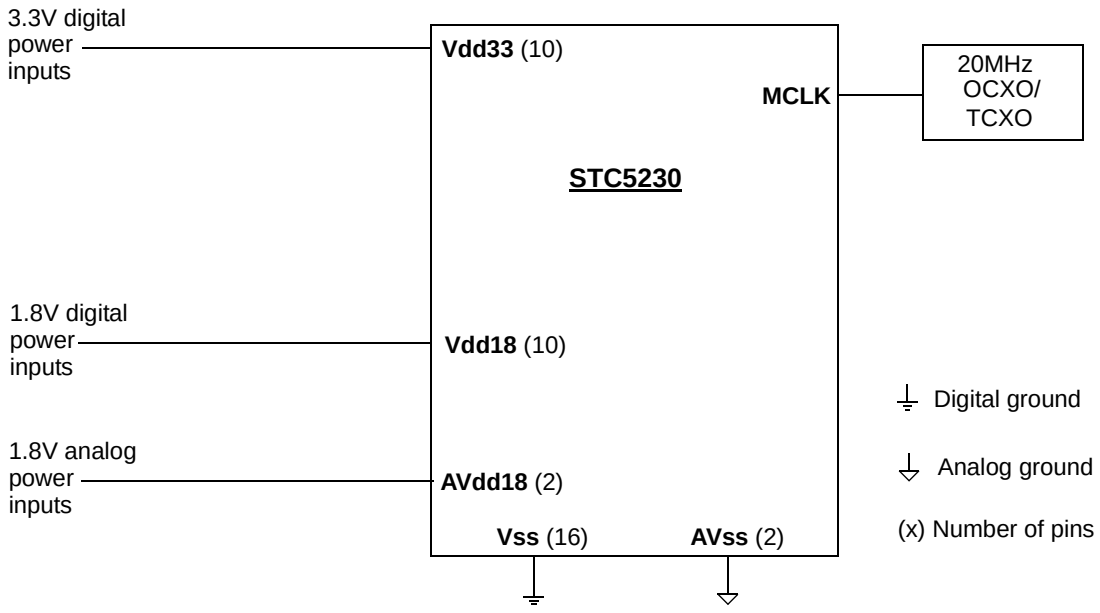
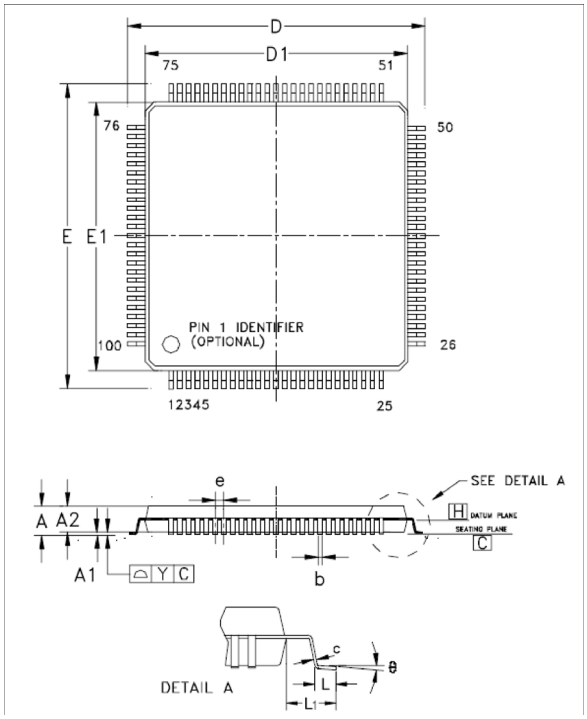


Figure 14: Powers and Grounds

The external 20MHz TCXO/OCXO master oscillator is connected to the **MCLK** pin.

Mechanical Specifications



Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		16.00	BSC		0.630	
E		16.00	BSC		0.630	
e		0.50	BSC		0.020	
D1		14.00	BSC		0.551	
E1		14.00	BSC		0.551	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00	REF		0.039	
Y		0.08			0.003	
θ	0°	3.5°	7°	0°	3.5°	7°

Controlling dimensions are in millimeters

Ordering Information

Part Number	Description
STC5230	Commercial Temperature Range Model
STC5230-I	Industrial Temperature Range Model

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
P01	Initial issue	

For more information, contact:

CONNOR WINFIELD

2111 Comprehensive DR
Aurora, IL. 60505, USA
630-851-4722
630-851-5040 FAX
www.conwin.com